

Development of a Multi-Bus, Multi-Source Reconfigurable Stirling Radioisotope Power System Test Bed

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The National Aeronautics and Space Administration (NASA) has typically used Radioisotope Thermoelectric Generators (RTG) as their source of electric power for deep space missions. A more efficient and potentially more cost effective alternative to the RTG, the high efficiency 110 watt Stirling Radioisotope Generator 110 (SRG110) is being developed by the Department of Energy (DOE), Lockheed Martin (LM), Stirling Technology Company (STC) and NASA Glenn Research Center (GRC). The SRG110 consists of two Stirling convertors (Stirling Engine and Linear Alternator) in a dual-opposed configuration, and two General Purpose Heat Source (GPHS) modules. Although Stirling convertors have been successfully operated as a power source for the utility grid and as a stand-alone portable generator, demonstration of the technology required to interconnect two Stirling convertors for a spacecraft power system has not been attempted. NASA GRC is developing a Power System Test Bed (PSTB) to evaluate the performance of a Stirling convertor in an integrated electrical power system application. This paper will describe the status of the PSTB and on-going activities pertaining to the PSTB in the NASA Thermal-Energy Conversion Branch of the Power and On-Board Propulsion Technology Division.

Nomenclature

DAS	Data Acquisition System
DOE	Department of Energy

FPGA Field Programmable Gate Array
GPHS General Purpose Heat Source
GRC Glenn Research Center
GPIB General Purpose Interface Bus

I/O Input-Output IP Internet Protocol

ISO / OSI International Standards Organization/Open Systems Interconnection

LMA Lockheed Martin Aeronautics

Mpbs Mega-bits-per-second

NASA National Aeronautics and Space Administration

PMAD Power Management and Distribution

PSTB Power System Test Bed

RISC Reduced Instruction Set Computer

RPC Remote Power Controller

RTG Radioisotope Thermal-electric Generators

SEU Single Event Upset

SRG110 Stirling Radioisotope Generator 110 Watt electric

STC Stirling Technology Company

TDC Technology Demonstration Convertors
UART Universal Asynchronous Receiver Transmitter

TCP Transmission Control Program

TCP/IP Transmission Control Program/Internet Protocol

I. Background

Design of spacecraft electrical power distribution systems vary depending on the intended mission, duration, number and types of loads and electrical sources of energy. Typical power sources may be solar (photovoltaic), battery, or thermoelectric. The selection of energy source is driven by the mission objectives, orbits, and paths of travel in relationship to the sun. Missions extending great distances from the sun (typically beyond the orbit of Mars) require extended-life energy sources, which, depending on the mission requirements, generally eliminate photovoltaic and battery technologies from consideration. Radioisotope based power sources become the logical choice for this class of missions. As currently conceptualized, Stirling radioisotope power convertors show the potential for higher efficiency than radioisotope thermoelectric generators; thereby producing the same amount of electrical power while using a smaller quantity of the radioisotope heat source.

Design and development of a Power Management and Distribution (PMAD) system suitable for interconnection of one or more Stirling power convertors for spacecraft, satellite or rover applications have not previously been attempted. In order to fully evaluate the performance of Stirling power convertors in a variety of applications, a Power System Test Bed (PSTB) is being developed. The test bed will allow many aspects of Stirling power convertor system integration to be investigated. Some of the areas that will be investigated are as follows: interconnection of single and multiple Stirling power convertor sources, evaluation of the performance of Stirling power convertors while connected to a variety of different load types, evaluation of different Stirling controller types, reduction of risks and performance improvement through extensive fault testing and design improvement, and determination of stability margins.

In order to realize the final working PMAD system design, both power distribution system architectures and control system architectures were developed. Prior to initiation of the design of the power distribution system architecture a survey was conducted of prior interplanetary missions. The data, when available, were organized by mission, year launched, nominal and peak electrical power output, types and number of energy sources, and the types and quantities of connected loads. This data was used to characterize the types of loads that could be expected for future missions.

The PSTB is designed to be highly flexible, allowing connection and management of multiple sources and loads. This will enable evaluation of the performance of different Stirling power convertors in a variety of configurations, rather than that of a single mission or application of Stirling power convertors. To protect the Stirling power convertors from excessive electrical loading, the Remote Power Controller (RPC) was developed. The RPC will provide precise control of load currents sensing and interruption of faults, without the latencies associated with conventional fuses.

The Technology Demonstration Convertor (TDC) is being developed by Stirling Technology Company (STC), previously under contract to Department of Energy (DOE), and currently under contract to Lockheed Martin Astronautics (LMA). There have been a total of 16 demonstrators built by STC to date. Glenn Research Center (GRC) has six of these in the Stirling Research Laboratory; four that were purchased for in-house testing and two that are being tested for LMA. Demonstrators #13 and #14 have been put on test for LMA at GRC in support of the SRG110 project (Fig. 1). These units are in operation around-the-clock and presently have been in operation in excess of 8200 hours.

II. Three Phases of Power System Test Bed Design

The build-up of the PSTB will be performed in three phases. Phase I will

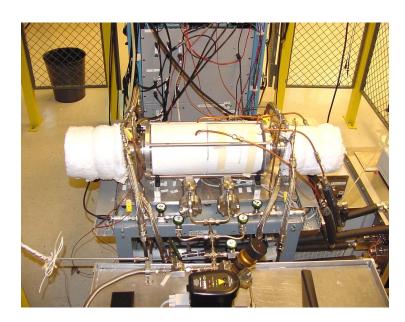


Figure 1. Technology Demonstrator Convertors #13 and #14 undergoing test at GRC.

have single power distribution bus architecture. Phase II will add a second power distribution bus, and additional Stirling convertor sources and loads. Phase III will add additional sources of power (battery and photovoltaic simulators) to the distribution system. Each phase will address different performance areas.

A. Phase I

Phase I is a single bus power system architecture (Fig. 2) and will consist of a single bus connected to a pair of Stirling convertors. Different Stirling power convertors and controller combinations operated one at a time are connected to multiple loads. The input to the power distribution system will be the shunt regulated output of the Stirling controller. Electrical energy (AC) produced within the linear alternator is rectified and shunt regulated by the controller. Convertors are arranged as dual-opposing pairs. A benefit of arranging the convertors in this manner is dynamic balancing of the free pistons.

Loads will be fixed and programmable in the PSTB by utilizing a programmable electronic load (NH Research S300) capable of constant current, constant voltage, constant resistance and constant power with a transient generator (40 microseconds – 1 second period and 10 microseconds – 1 second Rise/Fall time). The initial Stirling power convertors to be operated with the PSTB will be the STC TDC and Sunpower Incorporated EE-35 Stirling convertors. These Stirling power convertors are located in the Stirling Research Laboratory that was established to support a wide variety of tests related to the performance of Stirling power convertors. The PSTB will use Stirling convertors as the primary source of electrical power. The Stirling piston stroke and linear alternator power output of the TDC is controlled by a zener diode referenced, shunt regulated controller. Since the nominal output of the Stirling convertor pair is approximately 90 volts DC after the shunt regulator, and a nominal bus voltage of 28 volts DC is desired, DC/DC conversion will be used to reduce the output voltage. Other test configurations are planned, using a digital power controller with power factor correction.

Output power of each TDC convertor is nominally 55 watts electric (We) or 110We for the pair. The convertors are designed to operate at nominal temperatures of 650 °C hot end and 80 °C cold end. The goals of this development phase include demonstration of performance, response to transients, and stability margin while operating a variety of connected loads. The PSTB design will be augmented as necessary in order to satisfy these goals. Stirling power convertor control schemes include zener diode controlled shunt regulated and advanced solid state controllers featuring active power factor correction.

Phase I development of the PSTB will encompass multiple areas of technology development and engineering design. The technology development areas are: Stirling power convertor analysis, PMAD system analysis, component testing, and subsystem integration. The engineering design areas involve: systems requirements

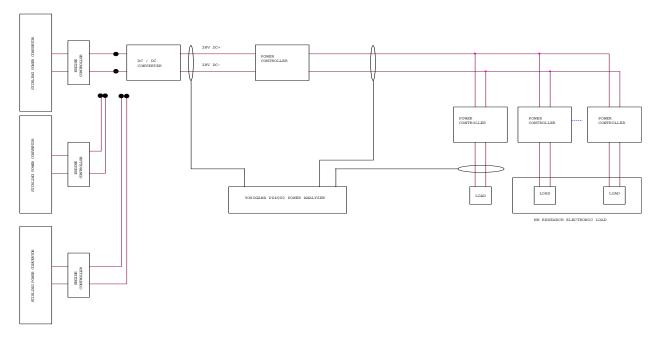


Figure 2. Power system architecture of Phase I.

definition, component selection, prototype development, performance testing, and control software and embedded firmware requirements definition, development and implementation.

In order to better understand the convertor performance with different configurations and loads, an analysis of both the PMAD and control system is being performed. Portions of the electrical power distribution system are being simulated using PSpice, and end-user power quality and system performance will be reviewed. The test results of the Stirling convertor configurations will then be compared to the analyses and predictions.

B. Phase II

The second phase of PSTB development will again incorporate multiple Stirling convertors to provide electrical power to the PSTB, this time with multiple primary power busses. The additional electrical busses add the capability to perform automated switching of critical loads to alternate power sources in the event of the loss of a primary electrical source. The design of the PSTB is such that it may be reconfigured electrically to allow the connection of multiple sources and loads to facilitate the evaluation of the Stirling power convertors under a variety of system configurations.

Loads designated as system critical may be fed from multiple busses, configured to select a second energized bus in the event of the loss of the primary bus. Multiple Stirling power convertors will be connected and power the separate busses.

C. Phase III

Phase III will incorporate photovoltaic and battery simulators operating in conjunction with Stirling power convertors, simulating a spacecraft power bus. Control hardware representative of a flight system will be developed and integrated into the system, and loads representative of recent flight missions will be incorporated. For example, the RPC microcontroller will be integrated into a Single Event Upset (SEU) radiation-hardened Field Programmable Gate Array (FPGA). System operational profiles will be developed that are more like those of a multi-mission spacecraft.

III. Remote Power Controller (RPC) Development

The Stirling convertor power sources must be protected from excessive electrical loading of their alternator outputs. This will be accomplished via active load management by the RPC and the control computer of the PMAD system. Loads that draw currents in excess of their assigned values will cause their respective power controller to first limit the current, then open the circuit, interrupting the load current. Fault protection will be accomplished in the same manner by isolating the fault as close as possible to the source of the fault. This will be accomplished by careful programming of the trip points of the power controllers throughout the PMAD system. The use of solid state power relays in conjunction with high-side current monitoring enables more precise control of load currents sensing and interruption of faults. This method of over-current monitoring alleviates the latencies associated with conventional I²T trip curves used in fuses. The system will consist of multiple power controllers, connecting user electrical loads to primary power distribution busses. To improve fault tolerance, the PMAD system will be modified to incorporate non-critical load shedding and critical load connection to available active power sources. This functionality will be investigated in Phase II of the Stirling Engine PSTB construction.

The RPC is being developed at GRC. The RPC is a new design, incorporating a high-speed Reduced Instruction Set Computer (RISC) microcontroller operating in conjunction with an embedded Ethernet interface. A high-side current monitor and voltage divider at the input of the RPC supply the microcontroller with load current and load voltage. The microcontroller sends a signal to a solid state relay, and receives relay status back. The RPC is used throughout the power system design to support the management and distribution of electrical power.

As stated earlier, the RPC (Fig. 3) facilitates the automated remote control of the solid state relay via an embedded device server. The RPC consists of the solid state relay, a microcontroller (Atmel ATmega16®), a current monitor, an embedded device server Ethernet interface (Lantronix X-port®), interface electronics between the relay and microcontroller, and a voltage monitor. The solid state relay selected for this application is a Teledyne Relay LD22CMW. It is a 10 Ampere relay with short-circuit protection and switch status output. It was selected for its reliability, self protection, and switch status output. The nominal "on" resistance of the solid state relay is 0.1 ohms. The low resistance reduces the voltage drop across the solid state relay, thus conserving energy. The

microcontroller will provide direct command and control of the solid state relay while monitoring load current and voltage.

Current monitoring is facilitated by a "high-side" current monitoring amplifier circuit (Maxim MAX4080SASA). The high side current monitor has a high (76 Volt DC) common mode range and is not subject to measurement errors produced by ground faults in the return path of the circuit. Should the load current exceed a predefined threshold, the microcontroller will command the relay to open the load current path. A follow-on design will incorporate load current reduction prior to opening the solid state relay, and utilize a high-side power controller with internal current monitoring, thus significantly reducing the controller parts count. The microcontroller is serially interfaced to the embedded device server. The firmware controls the microcontroller Input-Output (I/O) ports that interface to the solid state relay and the Universal Asynchronous Receiver Transmitter (UART) that interfaces serially to the X-port Ethernet interface. Commands will originate at the host computer and be transmitted via Ethernet at 100 Mbps to each individual power controller Ethernet interface. The Ethernet interface communicates asynchronously to the microcontroller, delivering instructions and receiving relay status and telemetry data. The embedded device server selected for this application is a Lantronix X-port. The device server contains the Transmission Control Program/Internet Protocol (TCP/IP) stack and provides the complete device server communication through a Transmission Control Program (TCP) data channel, telnet connection or via a web server.

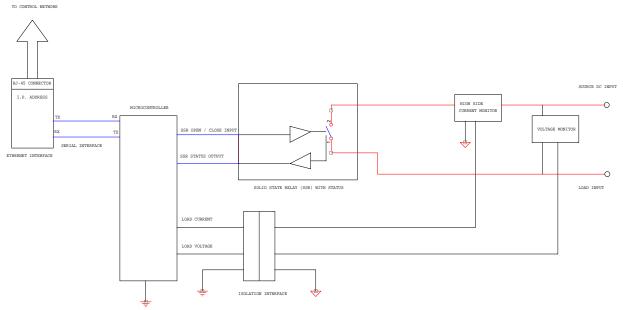


Figure 3. Remote Power Controller block diagram.

To satisfy the increased reliability requirements of a flight system, a second power switch may be incorporated in the return leg of the load to provide complete load isolation. The manufacturer of the microcontroller produces a radiation hardened FPGA with built-in SEU protection for space applications. In the event that the solid state power controller design is utilized for space flight, the functionality of the microcontroller could be implemented onto a radiation hardened FPGA to meet the radiation requirements of the space application.

IV. PMAD System Performance Testing

There are a number of performance metrics by which the power system will be evaluated. In order to ensure adequate power quality to the end user, a number of system level tests will be conducted. If the PMAD system design fails to meet established design goals it will be iterated as necessary to achieve the desired level of

performance. Initial testing will utilize a programmable electronic load with a wide range of resistive loads and durations. This will enable evaluation of the system performance during both steady-state and transient loading. The predicted results will be documented in the test plans and procedures. Each plan and procedure will be reviewed and approved as a guideline for each PSTB test activity.

The current plan is to evaluate and demonstrate the following functions on the Phase I PSTB:

- Electrical power system integration to the Stirling convertor,
- Electrical power system stability margin at steady state,
- Electrical power system stability margin during and after transient load conditions, and
- System ability to operate with lagging Power Factor (PF) loads

V. Control System Architecture

The communication bus enables command, control, and monitoring of the power switching elements. Figure 4 illustrates the control system architecture for Phase I of the PSTB overlaid on the power system architecture. The control computer communicates using TCP/IP over a computer network via Ethernet to each RPC. The Ethernet bus was selected because of the availability of software tools, many of which are built-in on most desk top computer systems or are readily available. More recently, embedded systems suppliers have significantly reduced the size of Ethernet host interfaces while increasing the standard bus speed to 100 Mega-bits-per-second (Mbps). Networking components are being developed that have the data capacity of 1 Giga-bits-per-second throughput. Internet Protocol (IP) is a connectionless (no physical connection between transmitter and receiver) best effort delivery system. The IP provides a virtual network across multiple physical networks providing a routing mechanism that directs datagrams (data packets, Fig. 5) directly or indirectly across the network. The data portion of the data frame carries information on the RPC current, voltage and relay position. It also carries command data for a particular RPC from the Control Computer. The protocol contains built in mechanisms for handling errors resulting from unreachable hosts or non-existent destination addresses. In this application, care has been taken to ensure that traffic flow on the data network will be exclusive to this system, and not linked to other computer data networks. By isolating the network data from other data traffic, congestion on the data network (reducing system performance) can be avoided. This will ensure maximum throughput between the control computer and the individual remote hosts at each solid state power controller.

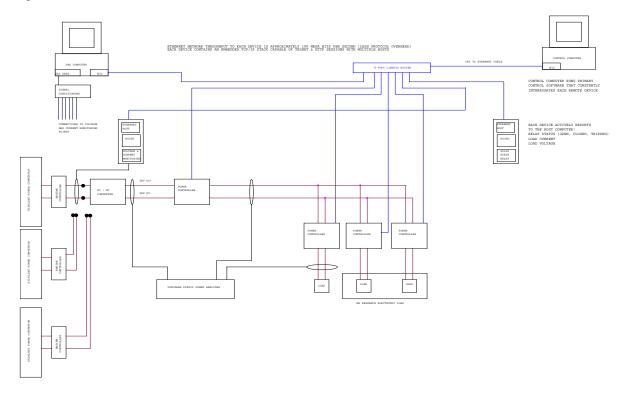


Figure 4. Control system architecture of phase I.

This system communicates using TCP/IP and follows the International Standards Organization/Open Systems Interconnection (ISO/OSI) reference model.² The solid state relay controller interfaces to the Ethernet host at the physical layer (hardware) of the TCP/IP stack. The "stack" is a reference to the ISO/OSI 7 layer protocol. The TCP/IP stack facilitates rapid communication between the microcontroller controlling the solid state relay and the control computer. In this configuration the microcontroller and Ethernet interface form a data server and the control computer is the client requesting status from the data server. The requested status contains the present status of the solid state relay (open, closed, and tripped), load voltage, and load current. Because the communications network ties the control computer to the solid state relay's embedded controller, it plays a key part in establishing the overall performance of the control system. Many issues associated with the control network implementation play a key role in the resulting system performance. Statistics about this packet-based data flow (packet loss rate, forwarding rate, and throughput) indicate the loading of the network and the resulting performance of the network. Figure 5 shows the breakdown of a typical Ethernet packet. Quantitative decisions can be made about the overall adequacy of the communication system performance.

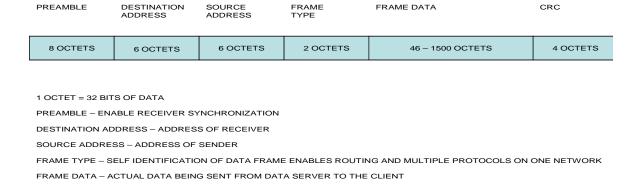


Figure 5. Breakdown of a typical Ethernet packet.

CRC - CYCLIC REDUNDANCY CHECK - ERROR CHECKING OF THE FRAME

VI. Data Acquisition System and Programmable Load

The PSTB is managed by the Control Computer which obtains near real-time measurement data from the RPC microcontroller via the control data network. Measurements made at each RPC during operation are made available to the Control Computer. A Data Acquisition System (DAS) will record voltages and currents throughout the power distribution system at the sources. This system will operate independently from the data collection system of the PMAD system. Measurement data is collected by the DAS in real time during operations and stored for later analysis. The purpose of the DAS is to give an independent verification of the measurement data reported by the PSTB Control Computer. Additionally, the DAS can be programmed to sample many times higher than the sample rate of the PSTB control system, enabling high definition data during transient electrical events. The DAS computer will be triggered over the computer network from the Control Computer, synchronizing the two data systems. The DAS system will be programmed for automatic post-processing of test data to reduce user workload. A graphics package (Origin) has been incorporated in the DAS that will automate graphing and management of test data.

The programmable load is controlled via a General Purpose Interface Bus (GPIB) and will interface to the DAS computer. The DAS computer can be used to transfer load profiles to the programmable load and then await commands from the Control Computer to execute a specified profile during system operation. Data gathered from this testing will be useful for testing and evaluating a system powered by Stirling convertors with various load profiles. Furthermore, by executing programmed load profiles it will be possible to compare different Stirling power convertors in different configurations over identical load conditions.

VII. Conclusion

The previous discussion provided both a system level overview and a detailed look at the key components of the Stirling convertor PSTB system design as well as the planned usage. The computer controls, communications network, power controls and their embedded firmware have been described. These elements work together at multiple operational levels in order to enable the rapid delivery of managed power to user loads, achieving the desired level of power quality. The advantages of this design are its simplicity, the reduced parts count, the increased reliability, and the use of many off-the-shelf components. The present plans are to utilize a high-side power switch containing an internal current monitor with feedback and load current reduction. This will enhance the Stirling convertor power controller performance by quickly isolating faults and utilizing current reduction to loads that exceed specified limits. Two power switches (both high- and low-side) will be implemented to enable complete isolation of critical loads, improving system reliability. By embedding the key control elements at the solid state power controller, independent operation may be facilitated at the lowest system level, thereby reducing response time and improving overall system performance. Some of these improvements are planned for the second generation power controllers and will be incorporated in the second phase of this project.

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13. ABSTRACT (Maximum 200 words)

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